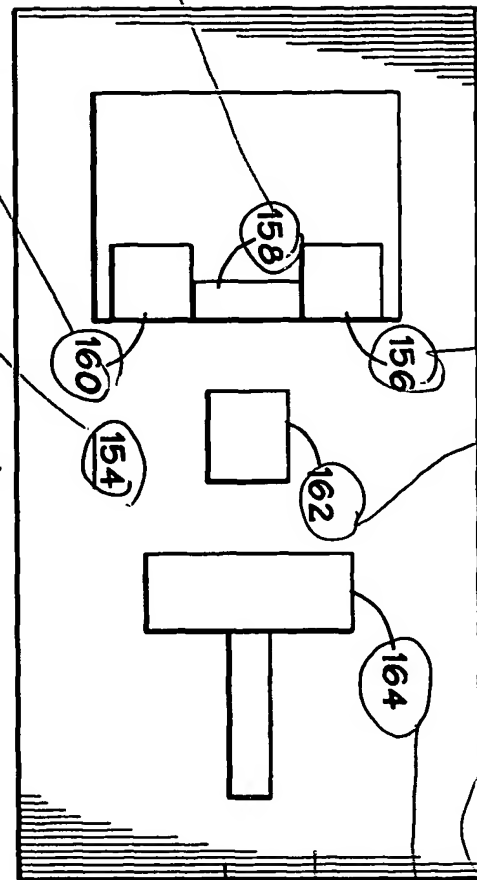


FIG. 4



channel

drain

gate

spacers

FIG. 6

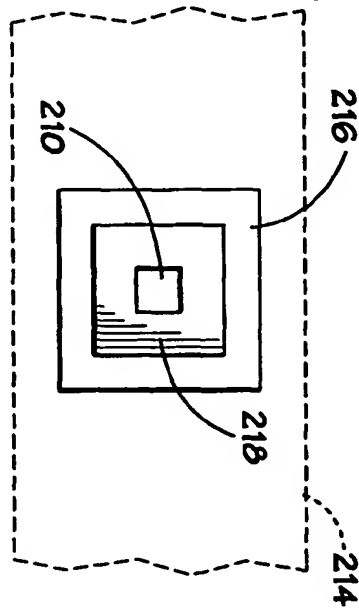
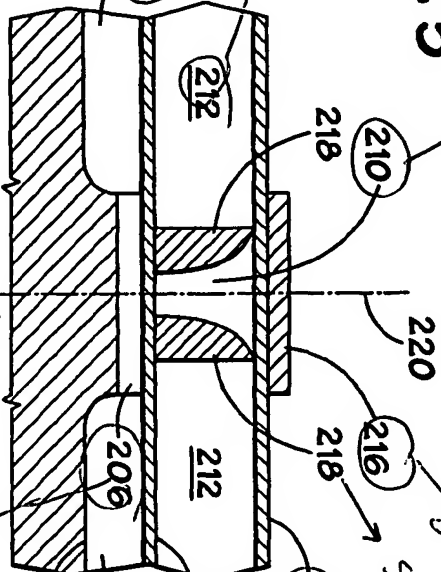


FIG. 5



dielectric

channel

substrate

vertical tunneling transistors

quantum dots

substrate

horizontally clipped tunneling transistor

gate

top view

prior art (known)